#24 | Reply Brief
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Tinku Acharya, et al.	§	Group Art Unit:	2625
Serial No.:	09/390,255	§	Examiner:	Timothy M. Johnson
Filed:	September 3, 1999	§		
For:	Wavelet Zerotree Coding of Ordered Bits	§	Atty. Dkt. No.:	ITL.0210US (P7057)

8/17/04

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

REPLY BRIEF

Noted 9-9-04

Dear Sir:

Applicant submits the following reply to the Examiner's Answer.

I. GROUPING OF THE CLAIMS

Claims 16-22 are grouped together; claims 23-28 are grouped together; and claims 29-33 are grouped together.

Date of Deposit: July 28, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to Mail Stop **Appeal Brief-Patents**, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.
Janice Munoz
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II. REPLY TO EXAMINER'S ARGUMENTS

The Examiner fails to show where Zandi allegedly teaches or suggests coding bits *to indicate zerotree roots that are associated with the bit order.* (*emphasis added*). Instead, the Examiner selectively pieces together different parts of Zandi to allegedly show the claim limitations. However, the Examiner's arguments are misleading. More specifically, Zandi does discuss wavelet coefficients, zerotree encoding and bitplanes. However, Zandi fails to teach or suggest coding bits of the wavelet coefficients to indicate zerotree roots that are associated with a particular bitplane.

Instead of providing such a teaching or suggestion, Zandi teaches using the bitplanes to test the significant of a particular wavelet coefficient and zerotree encoding the coefficient to indicate zerotree roots for the coefficient, not for the bitplane. The Examiner relies on the language found in lines 19-23 and 36-40 of col. 23 and lines 26-31 of col. 24 of Zandi to support the contention that Zandi allegedly teaches that bits are encoded to indicate zerotree roots for the bitplane. Examiner's Answer, 14. However, this conclusion is not supported by the cited language.

More specifically, in lines 19-23 of col 23 Zandi generally teaches that coefficients may be encoded to indicate an isolated zero or a zerotree root and in lines 36-40 of the same column, Zandi states that higher order bitplanes consist mostly of insignificant coefficients. Neither passage, however, teaches or suggests coding bits to indicate zerotree roots for the bitplane. Lines 26-31 of col. 24 of Zandi states that "coefficients are coded in a bit significance, or bit-plane embedded system." However, neither the mere presence of bit planes nor the mere disclosure that bit planes are used for purposes of determining coefficient significance teaches or suggests the missing claim language.

Furthermore, the Examiner fails to show where the missing claim limitations are taught or suggested by Kolarov. Instead, the Examiner points out similar terms in Zandi and Kolarov that appear to correspond to isolated words in the claim language. However, the combination of Zandi and Kolarov fails to teach or suggest the subject matter defined by claims 16-33 when the claim language is considered in its entirety.

Therefore, Applicant maintains that the §103 rejections of claims 16-33 are in error and should be reversed.

Respectfully submitted,

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APPENDIX OF CLAIMS

The claims on appeal are:

16. A method comprising:

providing wavelet coefficients that indicate an image, the bits of each wavelet coefficient being associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient; and

for each said bit order, coding the associated bits to indicate zerotree roots that are associated with said bit order.

17. The method of claim 16, wherein each bit order is associated with only one of the bits of each wavelet coefficient.

18. The method of claim 16, wherein the act of coding the bits comprises:

determining which of the bits indicate zeros; and

classifying each zero as either an isolated zero or a zerotree root.

19. The method of claim 18, wherein some of the wavelet coefficients are descendants of some of the other wavelet coefficients, and wherein the act of determining comprises:

traversing a descendant tree from a bit associated with one of said some of the wavelet coefficients to bits associated with said other wavelet coefficients to locate the zerotree roots.

20. The method of claim 16, wherein the act of providing comprises:

producing different levels of the code, each level being associated with a different resolution of the image.

21. The method of claim 20, wherein the levels that are associated with lower resolution are associated with higher orders.

22. The method of claim 16, wherein the act of providing wavelet coefficients comprises:

providing intensity level coefficients that indicate pixel intensities of the image; and

transforming the intensity level coefficients into wavelet subbands.

23. An article comprising a storage medium readable by a processor-based system, the storage medium storing instructions to cause a processor to:

provide wavelet coefficients that indicate an image, the bits of each wavelet coefficient being associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient; and

for each said bit order, code the associated bits to indicate zerotree roots that are associated with said bit order.

24. The article of claim 23, wherein each bit order-is associated with only one of the bits of each wavelet coefficient.

25. The article of claim 23, the storage medium comprising instructions to cause the processor to:

determine which of the bits indicate zeros, and

classify each zero as either an isolated zero or a zerotree root.

26. The article of claim 25, wherein some of the wavelet coefficients are descendants of some of the other wavelet coefficients, the storage medium comprising instruction to cause the processor to:

traverse a descendant tree from a bit associated with one of said some of the wavelet coefficients to bits associated with said other wavelet coefficients to locate the zerotree roots.

27. The article of claim 23, the storage medium comprising instructions to cause the processor to:

produce different levels of the code, each level being associated with a different resolution of the image.

28. The article of claim 27, wherein the levels that are associated with lower resolutions are associated with higher orders.

29. A computer system comprising:

a processor; and

a memory storing a program to cause the processor to:

provide wavelet coefficients that indicate an image, the bits of each wavelet coefficient being associated with a different bit order so that each bit order is associated with one of the bits of each wavelet coefficient; and

for each said bit order, code the associated bits to indicate zerotree roots that are associated with said bit order.

30. The computer system of claim 29, wherein each bit order is associated with only one of the bits of each wavelet coefficient.

31. The computer system of claim 29, wherein the program causes the processor to code the bits by determining which of the bits indicate zeros and classifying each zero as either an isolated zero or a zerotree root.

32. The computer system of claim 31, wherein some of the wavelet coefficients are descendants of some of the other wavelet coefficients, and wherein the processor determines which of the bits are zeros by traversing a descendant tree from a bit associated with one of said some of the wavelet coefficients to bits associated with said other wavelet coefficients to locate the zerotree root.

33. The computer system of claim 29, wherein the program causes the processor to provide the wavelet coefficients by producing different levels of the code, each level being associated with a different resolution of the image.